CLAIMS

What is claimed is:

1. An electrical device comprising:

first and second substrates, at least one having a semiconductor layer thereon; and

a bond structure bonding the first substrate to the second substrate, the bond structure including an alloy bonded to the semiconductor layer and composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed.

2. The electrical device as defined in Claim 1, wherein the oxide affinity material is not more than about half the weight of the alloy interfacing the semiconductor layer.

3. The electrical device as defined in Claim 1, further comprising electrical insulation, situated between the first and second substrates, for electrically isolating a plurality integrated circuits.

4. The electrical device as defined in Claim 1, further comprising a region having a closed environment between the first and second substrates, wherein the region is defined at least in part by the bond structure.

5. The electrical device as defined in Claim 1, further comprising a hermetically sealed region between the first and second substrates, wherein the hermetically sealed region is defined at least in part by the bond structure.

6. The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is sufficient to maintain an alignment of said first substrate with respect to the second substrate.

7. The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is composed of noble metal alloyed with an oxide affinity material having a free energy that is lower than that of silicon dioxide.

8. The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is composed of noble metal alloyed with a material having a free energy less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

9. The electrical device as defined in Claim 1, wherein the alloy bonded to the semiconductor layer is composed of noble metal alloyed with a material selected from the group consisting of Al, As, B, Ca, Ce, Co, Cr, Fe, Ga, Hf, In, La, Li, Mg, Mn, Nb, Nd, Ge, Pr, Sb, Si, Ta, Th, Ti, V, W, and Zr.

10. An electrical device comprising first and second semiconductor wafers each including a plurality of integrated circuits, wherein:

the first semiconductor wafer has a silicon layer thereon;

the silicon layer on the first semiconductor wafer is bonded to the second semiconductor wafer by gold alloyed with an oxide affinity material having an oxygen affinity higher than that of silicon.

11. The electrical device as defined in Claim 10, wherein the oxide affinity material makes up not more than about half the weight of the gold.

12. The electrical device as defined in Claim 10, wherein the silicon layer on the first semiconductor wafer has a native oxide layer thereon.

13. The electrical device as defined in Claim 10, further comprising a closed environment between the first and second semiconductor wafers that is defined in part by:

the silicon layer on the first semiconductor wafer; and

the gold alloyed with the oxide affinity material.

14. The electrical device as defined in Claim 10, further comprising a hermetically sealed region between the first and second semiconductor wafers that is defined in part by:

the silicon layer on the first semiconductor wafer; and

the gold alloyed with the oxide affinity material.

15. An electrical device comprising:

first and second semiconductor wafers each including a plurality of integrated circuits;

silicon on the first semiconductor wafer; and

a bonding structure including gold alloyed with a material having a free energy lower than that of silicon dioxide, wherein the first semiconductor wafer is bonded to the second semiconductor wafer by the gold alloy that is bonded to the silicon on the first semiconductor wafer.

16. The electrical device as defined in Claim 15, wherein the free energy of the material is less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

17. The electrical device as defined in Claim 15, wherein the material selected from the group consisting of Ti Al, Li, Mg, and Ca.

18. An electrical device comprising:

first and second substrates each including a plurality of integrated circuits and the first substrate having a semiconductor layer thereon;

a bonding structure having opposing ends respectively upon the semiconductor layer of the first substrate and the second substrate, the bonding structure including:

a noble metal base layer upon the second substrate;

an oxide affinity material in contact with the noble metal base layer and having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed; and

a noble metal interface between the oxide affinity material and the semiconductor layer, wherein the first substrate is bonded to the second substrate by the bonding structure.

19. The electrical device as defined in Claim 18, wherein:

the oxide affinity material has a thickness in a range from about 0.1 microns to not more than about 2 microns; and

the noble metal interface has a thickness not more than about two microns.

20. The electrical device as defined in Claim 18, wherein the oxide affinity material in contact with the noble metal base layer is selected from the group consisting of Al, As, B, Ca, Ce, Co, Cr, Fe, Ga, Hf, In, La, Li, Mg, Mn, Nb, Nd, Ge, Pr, Sb, Si, Ta, Th, Ti, V, W, and Zr.

21. The electrical device as defined in Claim 18, further comprising a region having a closed environment between the first and second substrates and defined in part by the bonding structure, wherein the plurality of integrated circuits are within the closed environment.

22. The electrical device as defined in Claim 21, wherein the closed environment is a hermetically sealed region.

23. The electrical device as defined in Claim 18, wherein the oxide affinity material in contact with the noble metal base layer has a free energy that is lower than that of silicon dioxide.

24. The electrical device as defined in Claim 18, wherein the oxide affinity material in contact with the noble metal base layer has a free energy less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

25. An electrical device comprising:

first and second semiconductor wafers each including a plurality of integrated circuits and the first semiconductor wafer have a silicon layer thereon;

a bonding structure having opposing ends respectively on the silicon layer and the second semiconductor wafer, the bonding structure including:

a gold base layer upon the first semiconductor wafer;

an oxide affinity material in contact with the gold metal base layer and having an affinity for oxygen higher than that of silicon; and

a gold interface between the oxide affinity material and with the silicon layer, wherein the first semiconductor wafer is bonded to the second semiconductor wafer by the bonding structure.

26. The electrical device as defined in Claim 25, wherein the oxide affinity material has a thickness in a range from about 0.1 microns to not more than about 2 microns.

27. The electrical device as defined in Claim 25, wherein the silicon layer has a native oxide thereon.

28. The electrical device as defined in Claim 25, further comprising a region having a closed environment between the first and second semiconductor wafers and defined in part by the bonding structure, wherein the plurality of integrated circuits are within the closed environment.

29. The electrical device as defined in Claim 28, wherein the closed environment is a hermetically sealed region.

30. An electrical device comprising first and second semiconductor wafers each including a plurality of integrated circuits enclosed within a sealed region that is defined in part by a bonding structure bonding the first semiconductor wafer to the second semiconductor wafer and including:

a silicon material;

a gold base layer upon the silicon material;

an oxide affinity material in contact with the gold metal base layer and having a free energy lower than that of silicon dioxide; and

a noble metal interface on the oxide affinity material.

31. The electrical device as defined in Claim 30, wherein the oxide affinity material has a free energy less than a range from about -200 Kcal/mol to about -205 Kcal/mol.

32. The electrical device as defined in Claim 30, wherein the oxide affinity material is selected from the group consisting of Ti Al, Li, Mg, and Ca.

33. An electrical device comprising first and second substrates bonded together with a first material having dispersed therein a reducing agent for the diffusion therein of oxidation of a second material of which at least one of the first and second substrates is composed, wherein the reducing agent has a higher affinity for oxygen than that of the second material

34. The electrical device as defined in Claim 33, wherein:

the first material comprises gold; and

the second material comprises silicon.

35. A substrate bonding method comprising bonding together a semiconductor layer on a first substrate to an alloy interface on a second substrate that is composed of noble metal alloyed with an oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed.

36. The method as defined in Claim 35, wherein the bonding together comprises the steps of:

co-sputtering the oxide affinity material with the noble metal upon native oxide on the second substrate; and

pressing the co-sputtered oxide affinity material and noble metal against a native oxide that is on the semiconductor layer on the first substrate, wherein during said pressing:

the native oxide that is on the semiconductor layer on the first substrate is diffused into the noble metal that contains the oxide affinity material and reacts with the dispersion of the oxide affinity material within the noble metal; and

the noble metal is alloyed with the oxide affinity material.

37. A substrate bonding method comprising bonding together a silicon layer on a first substrate with an alloy interface on a second substrate, the alloy interface being composed of noble metal alloyed with an oxide affinity material having a free energy that is lower than that of silicon dioxide.

38. The method as defined in Claim 37, wherein the bonding together comprises the steps of:

co-sputtering the oxide affinity material with the noble metal upon the second substrate; and

pressing the co-sputtered oxide affinity material and noble metal against a native oxide that is on the silicon layer on the first substrate, wherein during said pressing:

the native oxide on the silicon layer is removed by diffusing into the noble metal upon the second substrate and reacting with the oxide affinity material;

the noble metal is alloyed with the oxide affinity material; and

the first substrate is bonded to the second substrate.

39. The method as defined in Claim 38, wherein the pressing further comprises the step of forming the alloy interface so as to be sufficient to maintain an alignment of said first substrate with respect to the second substrate.

40. The method as defined in Claim 37, wherein the oxide affinity material is not more than about half the weight of the alloy interface.

41. The method as defined in Claim 37, further comprising, prior to the step of bonding together a silicon layer on a first substrate with an alloy interface on a second substrate, the step of forming a plurality of integrated circuits in at least one of the first and second substrates.

42. The method as defined in Claim 41, wherein:

the step of bonding together a silicon layer on a first substrate with an alloy interface on a second substrate forms a region having a closed environment between the first and second substrates; and

the plurality of integrated circuits in at least one of the first and second substrates are within the region having the closed environment

43. The method as defined in Claim 42, wherein the region having the closed environment is a hermetically sealed region.

44. The method as defined in Claim 37, wherein:

the noble metal comprises gold or a gold alloy; and

the oxide affinity material is selected from the group consisting of Al, As, B, Ca, Ce, Co, Cr, Fe, Ga, Hf, In, La, Li, Mg, Mn, Nb, Nd, Ge, Pr, Sb, Si, Ta, Th, Ti, V, W, and Zr.

45. The method as defined in Claim 44, wherein the oxide affinity material is selected from the group consisting of Ti Al, Li, Mg, and Ca.

46. The method as defined in Claim 37, wherein, prior to the bonding together a silicon layer on a first substrate with an alloy interface on a second substrate, the silicon layer on the first substrate has a native oxide thereon.

47. A substrate bonding method comprising the steps of:

forming a plurality of integrated circuits in at least one of first and second substrates;

forming a semiconductor layer on the first substrate;

forming a noble metal base layer upon the second substrate;

forming an oxide affinity material in contact with the noble metal base layer, the oxide affinity material having an affinity for oxygen higher than that of the material of which the semiconductor layer is composed;

forming a noble metal interface upon the oxide affinity material; and

pressing the semiconductor layer on the first substrate against the noble metal interface in order to:

remove a native oxide on the semiconductor layer by diffusion into the noble metal interface and reaction with the oxide affinity material; and

form a bond between the first and second substrates.

48. The method as defined in Claim 47, wherein the pressing further comprises forming the bond of the first substrate to the second substrates so as to be sufficient to maintain an alignment of said first substrate with respect to the second substrate.

49. The method as defined in Claim 47, wherein:

the oxide affinity material has a thickness in a range from about 0.1 microns to not more than about 2 microns; and

the noble metal interface has a thickness of not more than about two microns.

50. The method as defined in Claim 47, wherein, prior to the pressing, the semiconductor layer on the first substrate has a native oxide thereon.

51. The method as defined in Claim 47, wherein the pressing forms a region between the first and second substrates having a closed environment in which are situated the plurality of integrated circuits in at least one of first and second substrates.

52. The method as defined in Claim 47, wherein:

the material of which the semiconductor layer is composed comprises silicon;

the noble metal comprises gold or a gold alloy; and

the oxide affinity material is selected from the group consisting of Al, As, B, Ca, Ce, Co, Cr, Fe, Ga, Hf, In, La, Li, Mg, Mn, Nb, Nd, Ge, Pr, Sb, Si, Ta, Th, Ti, V, W, and Zr.

53. The method as defined in Claim 47, wherein the pressing forms a composite of:

the semiconductor layer;

the noble metal interface;

the oxide affinity material; and

the noble metal base layer.

54. The method as defined in Claim 53, wherein the composite further comprises the first substrate.

55. A surface bonding method comprising bonding surfaces together with a material having dispersed therein a reducing agent into which oxidation on at least one of the surfaces is diffused to remove the oxidation from the at least one of the surfaces during the bonding.

56. The method as defined in Claim 55, wherein the reducing agent is not more than about half the weight of the material that bonds the surfaces together.

57. The method as defined in Claim 55, further comprising, prior to the step of bonding, the step of forming a plurality of integrated circuits on at least one of the surfaces, wherein the bonding surfaces together forms a closed environment between the surfaces in which are situated the plurality of integrated circuits on at least one of the surfaces.

58. The method as defined in Claim 55, wherein:

the surface on which the oxidation is situated is composed of silicon;

the material that bonds the surfaces together comprises gold or a gold alloy; and

the reducing agent is selected from the group consisting of Al, As, B, Ca, Ce, Co, Cr, Fe, Ga, Hf, In, La, Li, Mg, Mn, Nb, Nd, Ge, Pr, Sb, Si, Ta, Th, Ti, V, W, and Zr.

59. The method as defined in Claim 58, wherein, prior to the bonding, the silicon surface has a native oxide thereon.